

Figure 1  
(Prior Art)

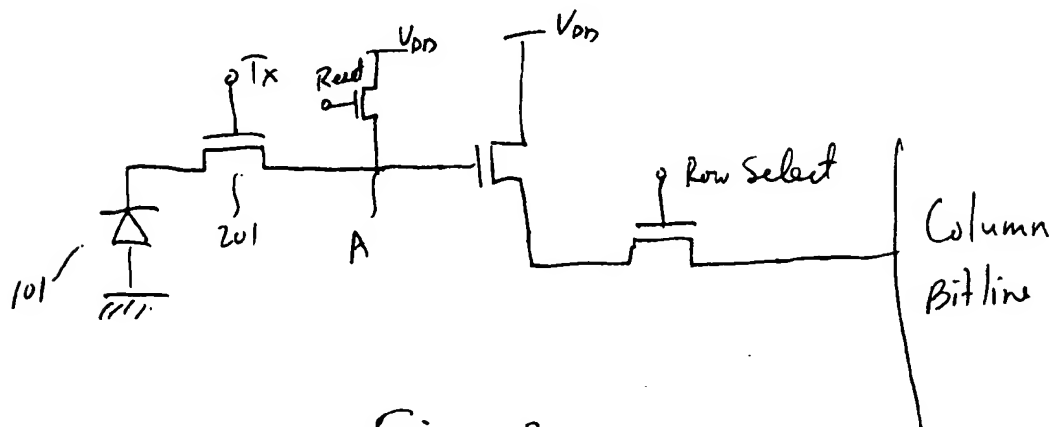


Figure 2  
(Prior Art)

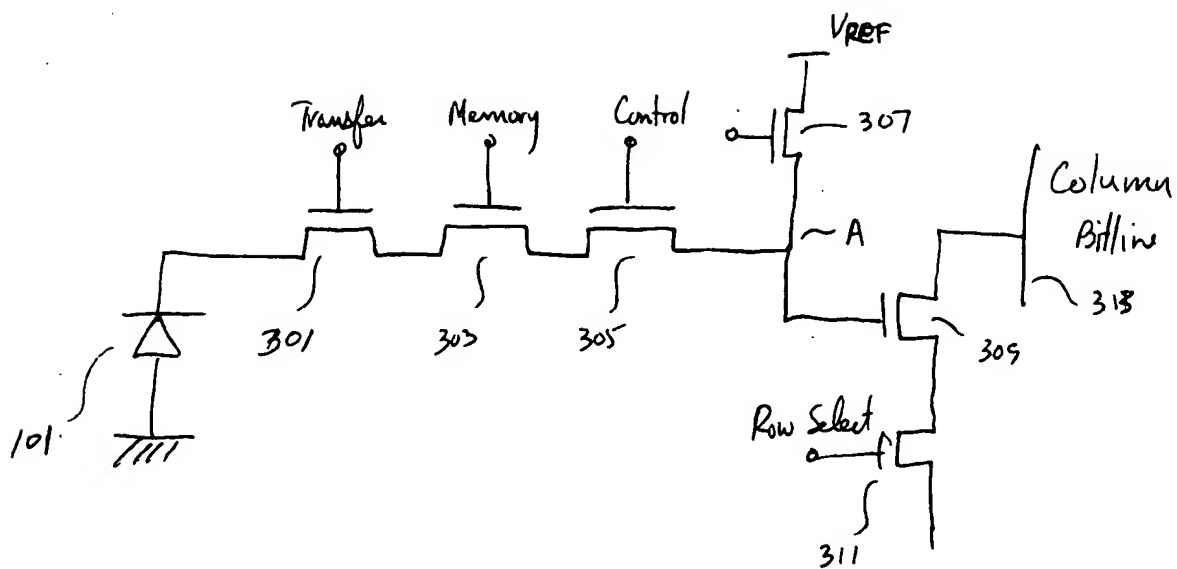


Figure 3

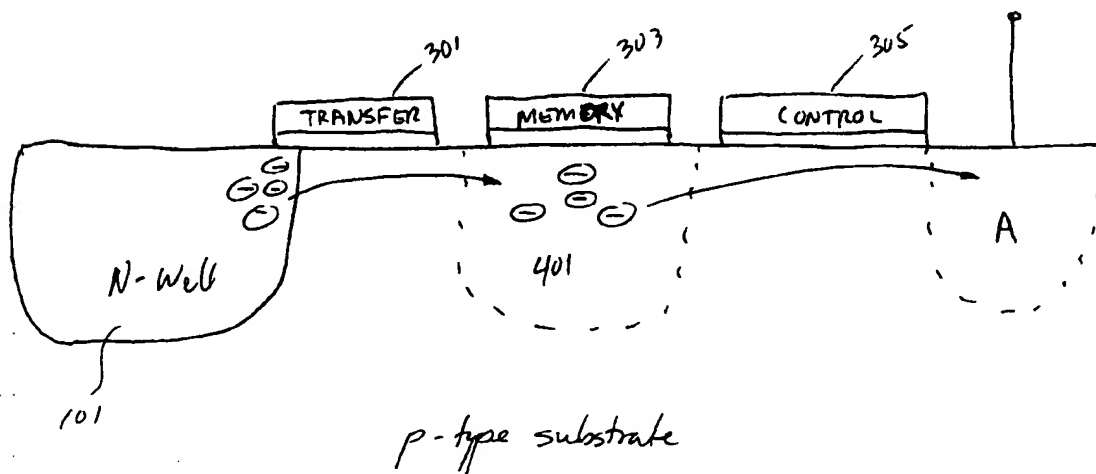
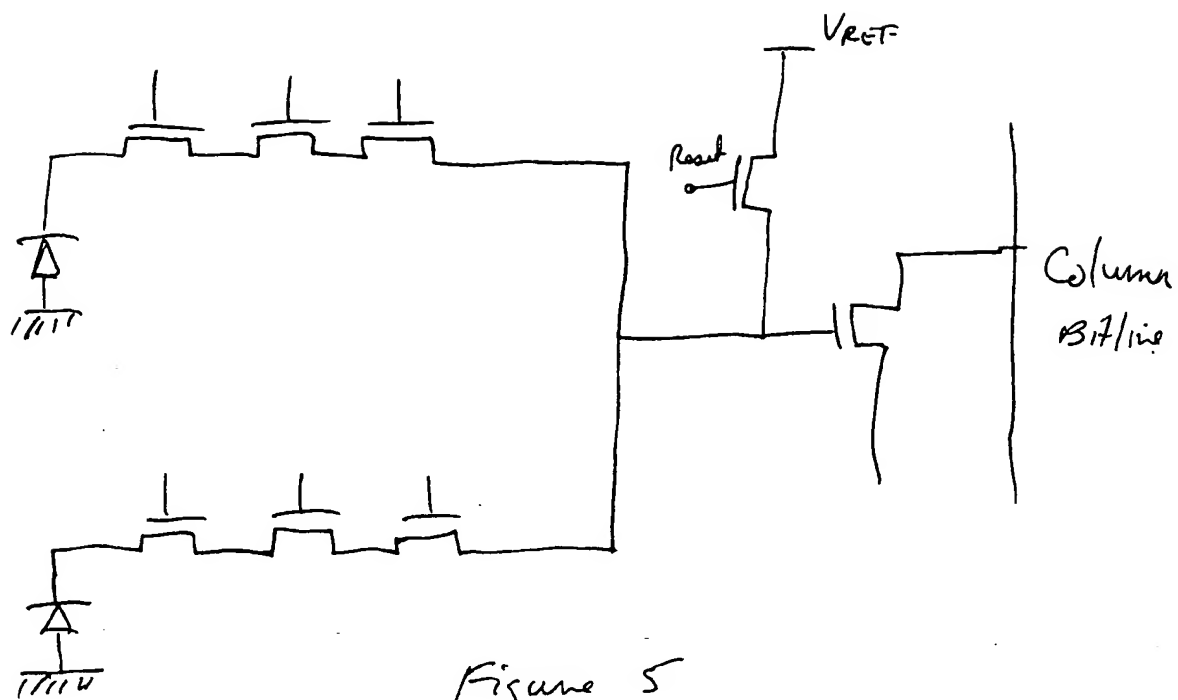


Figure 4



The diagram illustrates a 1T1R1C1P1M2G2A1S1F1R1G1 memory cell. It features a photodiode at the input, followed by a transfer gate, two memory gates (Gate 1 and Gate 2), a reset gate, and a control gate. The node between the control gate and the source follower is labeled 'A'. The source follower is connected to a column bitline, and the row gate is connected to Vdd.

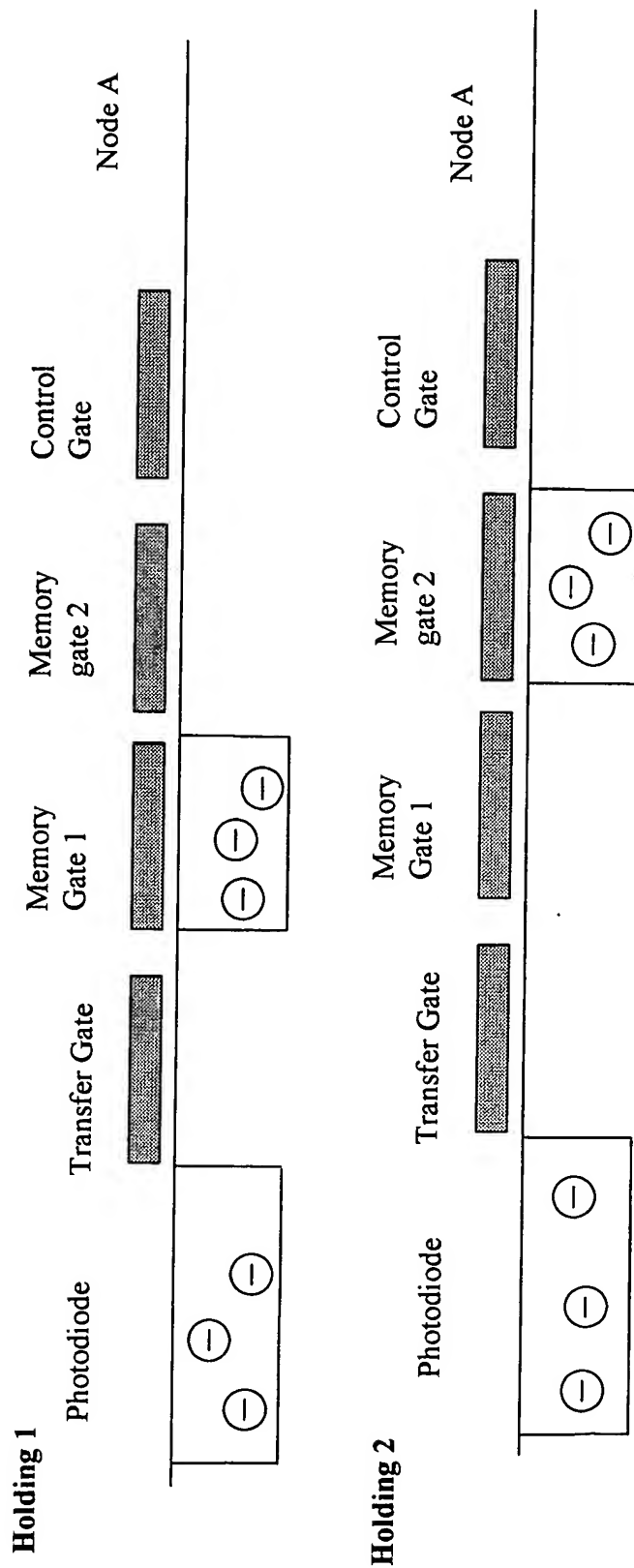


Figure 7

